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EXAMINER	
PARTRIDGE, WILLIAM B	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,756	RAUBUCH, MARTIN	
	Examiner	Art Unit	
	William B. Partridge	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 and 14-29 remain for examination

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 9, 14, 15, 17, 20, 22-27, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales, III et al. (U.S. Patent No. 5,996,057, herein Scales) in view of Agarwal et al. (U.S. Patent No. 5,758,176, herein Agarwal).

Claim 1 (amended)

Scales teaches: **An arrangement for vector permutation in a single-instruction multiple-data microprocessor, the arrangement comprising: a vector register file** (FIG. 2, Vector Register File 200); **a permutation logic block** (FIG. 2, Combine Network 210) **coupled to receive and permutate vectors from at least one vector register of the vector register file according to control parameters** (Column 2 lines 59-66, FIG. 2 *Note: Scales discloses performing a Permute-With-Replication operation on input vectors loaded into vector registers*) **the permutation of the vectors being as a side operation of an instruction** (Column 2 line 59 – Column 3 line 13, Column 4 line 49 – Column 6 line 14 *Note: The vector PWR instruction does not directly cause the vector operation to occur, the vector PWR instruction only specifies which*

registers to use and the registers themselves cause the PWR operation to occur and cause the operation to replicate without interaction of another instruction); **a plurality of control registers, each of the plurality of control registers being coupled to selectively provide control parameters to the permutation logic block** (Column 2 line 59 – Column 3 line 13, FIG. 2 *Note: Scales discloses using control vectors located in control registers to control the Permute-With-Replication operation*); **and a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.** (Column 2 line 59 – Column 3 line 13, Column 3 lines 3-4, FIG. 2 *Note: Scales discloses selecting a control vector and where the Permute-With-Replication operation is performed on the input vectors as specified by the control vector. The control register [as the control vector is contained within] used is specified by the operational code and as such there must inherently be some physical control means to select said specified control register as input to the PWR operation logic*).

Scales does not specifically teach: **control registers separate from the vector register file.**

However, Agarwal, in an analogous art, does teach the above limitation (FIG. 5 *Note: The control registers 244 are separate from the vector registers 236*). One of ordinary skill in the art would appreciate the use of control registers separate from the vector registers in order to allow alteration of control values independent of alteration of

data values, that is, to avoid bus contention and to provide a more modular design approach.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Agarwal into the teaching of Scales to have control registers separate from vector registers. The modification would have been obvious because one of ordinary skill in the art would have been motivated to avoid bus contention when needing to alter both control values and vector values and to provide a more modular design.

Claim 2 (amended)

Scales teaches: **A single-instruction multiple-data microprocessor vector permutation system comprising: at least one vector register;** (FIG. 2, Vector Register File 200) **a vector register file** (FIG. 2, Vector Register File 200); **a permutation logic block coupled to receive and permutate vectors from the at least one vector register of the vector register file according to control parameters** (Column 2 lines 59-66, FIG. 2 *Note: Scales discloses performing a Permute-With-Replication operation on input vectors loaded into vector registers*) **the permutation of the vectors being as a side operation of an instruction** (Column 2 line 59 – Column 3 line 13, Column 4 line 49 – Column 6 line 14 *Note: The vector PWR instruction does not directly cause the vector operation to occur, the vector PWR instruction only specifies which registers to use and the registers themselves cause the PWR operation to occur and cause the operation to replicate without interaction of another instruction*); **a plurality of control registers, each of the plurality of control**

registers being coupled to selectively provide control parameters to the permutation logic block (Column 2 line 59 – Column 3 line 13, Fig 2 *Note: Scales discloses using control vectors located in control registers to control the Permute-With-Replication operation*); **and a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block** (Column 2 line 59 – Column 3 line 13, Fig 2 *Note: See the rejection of claim 1*).

Scales does not specifically teach: **control registers separate from the vector register file.**

However, Agarwal, in an analogous art, does teach the above limitation (FIG. 5 *Note: The control registers 244 are separate from the vector registers 236*). One of ordinary skill in the art would appreciate the use of control registers separate from the vector registers in order to allow alteration of control values independent of alteration of data values, that is, to avoid bus contention and to provide a more modular design approach.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Agarwal into the teaching of Scales to have control registers separate from vector registers. The modification would have been obvious because one of ordinary skill in the art would have been motivated to avoid bus contention when needing to alter both control values and vector values and to provide a more modular design.

Claim 3 (amended)

The rejection of claim 1 is incorporated and further Scales teaches: **a negate block coupled to the controller and coupled to receive and selectively negate vectors from the permutation logic block according to the control parameters received from the controller, wherein the control parameters include permutation parameters and negate parameters** (Column 8 lines 32-33, Fig 6).

Claim 4 (amended)

The rejection of claim 1 is incorporated and further Scales teaches: **the controller includes at least one counter arranged to provide a sequential order for selecting one of the plurality of control registers** (Column 3 lines 11-13 *Note: Serially dependent functions require for operations to be performed sequentially. It is inherent that in order for progression of sequential order a counter of some kind must be present*).

Claim 5 (amended)

Claim 5 is the method claim corresponding to the apparatus claim 2 and is rejected under the same reason set forth in connection with the rejection of claim 2.

Claim 6

The rejection of claim 5 is incorporated and further Scales teaches: **the control register parameters are also used for determining negate characteristics and the step of permutating further includes the step of selectively negating the vectors according to the parameters of the selected control register** (Column 8 lines 32-33, Fig 6 *Note: A vector negation is a specific type of vector operation. The control*

parameters both create the control vector for the Permute-With-Replication operation and perform vector operations on the output vector).

Claim 7

The rejection of claim 5 is incorporated and further Scales teaches: **the step of selecting further includes the following of a sequential order of the plurality of control registers** (Column 3 lines 11-13 *Note: Serially dependent functions require for operations to be performed sequentially*).

Claim 9

The rejection of claim 4 is incorporated and further Scales teaches: **the sequential order includes automatic sequencing through a set of programmable control parameters** (Column 3 lines 3-5 *Note: Automatic sequencing is inherent in that the control vector can be the result of a computation previously performed*).

Claim 14

Claim 14 contains the same limitation as claim 3 and is rejected for the same reason set forth in connection with the rejection of claim 3.

Claim 15

Claim 15 contains the same limitation as claim 4 and is rejected for the same reason set forth in connection with the rejection of claim 4.

Claims 17 and 20

Claims 17 and 20 contain the same limitations as claim 9 and are rejected for the same reasons set forth in connection with the rejection of claim 9.

Claim 22

The rejection of claim 1 is incorporated and further Agarwal teaches: **the plurality of control registers is external to the vector register file** (FIG. 5)

Claim 23

The rejection of claim 1 is incorporated and further Agarwal teaches: **the vector register file is free of the plurality of control registers** (FIG. 5)

Claims 24-27

Claims 24-27 contain the same limitations as claims 22 and 23 and are rejected for the same reasons set forth in connection with the rejections of claims 22 and 23.

Claims 28-29

Claims 28-29 contain the same limitations as claims 1 and 2 and are rejected for the same reasons set forth in connection with the rejections of claims 1 and 2.

3. Claims 8, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales in view of Agarwal as applied to claims 1-7, 9, 14, 15, 17, 20, and 22-27 above, and further in view of Wang (U.S. Patent No. 6,886,124, herein Wang).

Claim 8

The rejection of claim 4 is incorporated and further Scales teaches: **the sequential order includes automatic sequencing** (Column 3 lines 3-5).

Scales does not specifically teach: **a set of fixed control parameters**

However, Wang, in an analogous art, discloses loading fixed values for use in a configuration sequence (Column 29 lines 57-59 *Note: Automatic sequencing is inherent in that the control vector can be the result of a computation previously performed*). One of ordinary skill in the art would appreciate the use of fixed control parameters in the use of commonly accessed parameters versus having to rewrite the parameters each time.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wang into the teaching of Scales to use fixed control parameters. The modification would have been obvious because one of ordinary skill in the art would have been motivated to have fixed values available to allow for faster access of commonly used parameters as opposed to having to program them over and over.

Claims 16 and 19

Claims 16 and 19 contain the same limitations as claim 8 and are rejected for the same reason set forth in connection with the rejection of claim 8.

4. Claims 10, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scales in view of Agarwal as applied to claims 1-7, 9, 14, 15, 17, 20, and 22-27 above, and further in view of Curry (U.S. Patent No. 4,935,891, herein Curry).

Claim 10

The rejection of claim 4 is incorporated but Scales does not specifically teach: **the sequential order is cyclical.**

However, Curry, in an analogous art, discloses the use of cyclical sequential order (Column 4 line 67 – Column 5 line 4). One of ordinary skill in the art would appreciate the use of a cyclical sequential order in order to repeat instructions to provide loop functionality.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Curry into the teaching of Scales to have cyclical sequential order. The modification would have been obvious because one of ordinary skill in the art would have been motivated to be able to easily repeat the same order of operations and to be able to implement loop functions.

Claims 18 and 21

Claims 18 and 21 contain the same limitations as claim 10 and are rejected for the same reason set forth in connection with the rejection of claim 10.

Response to Arguments

5. Applicant's arguments filed 1/21/2008 have been fully considered but they are not persuasive. Applicant argues in substance:

a. The Scales, III et al. patent does not possess separate features of a vector register file and a plurality of control registers as recited in Claim 1.

The control vectors of the Scales, III et al. patent are contained in the vector register file 200.

i. Examiner never asserted that Scales teaches separate registers, Examiner has relied upon Agarwal to teach the limitation.

b. However, if the skilled person were to combine the teachings of the cited Scales III et al. patent and the Agarwal patent, the resulting combination would fail to teach a plurality of control registers that are separate from a vector register file in combination with permutation of vectors as a side operation of an instruction according to control parameters provided by the plurality of control registers, as recited in Claim 1.

ii. Examiner respectfully disagrees. Agarwal establishes the use of a control register separate from the data registers (FIG. 5). Scales teaches that the permutation operation is an operation of an instruction (Column 2 line 59 – Column 3 line 13, Column 4 line 49 – Column 6 line 14). The claims do not require any specifics of the side operational status of the vector permutation operation. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant appears to argue further about the details of the side operational aspect of the vector operation. However, the specification

appears to contradict the arguments presented in regards to the side operation aspect. The specification, at page 4 lines 14-31, seems to suggest that the method of having the instructions be a side operation is not sufficient for programmer's needs for control over permutations. The vector operations are given additional functionality that would appear to require the vector operations to be their own instructions and not merely side operations. In the event the arguments regarding the claims were incorporated into the claims there would appear to be enablement issues.

Regardless, Applicant has openly admitted that it is known that permutation operations may be performed as side operations in the specification, at page 4 lines 14-18. As such, even if the limitations were incorporated then Applicant has admitted such limitations to be prior art and the claims could be rejected as such.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Examiner respectfully requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist Examiner in prosecuting the application.

8. When responding to this Office Action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William B. Partridge whose telephone number is (571) 270-1402. The examiner can normally be reached on M-F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner: William B. Partridge
Date: 2/5/08

EDDIE CHAN
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